CLAIMS:

1. Switch (20) comprising

- a first transistor (1) with main electrodes constituting in/outputs (Y,Z) of the switch (20) and with a control electrode constituting a first control input of the switch (20) for in response to a first control signal ("e") controlling the first transistor (1);
- a second transistor (2) with main electrodes constituting the in/outputs (Y,Z) of the switch (20) and with a control electrode constituting a second control input of the switch (20) for in response to a second control signal ("f") controlling the second transistor (2); and
- a circuit (21) for in response to the first control signal ("e") and an in/output signal ("y","z") at an in/output (Y,Z) of the switch (20) generating the second control signal ("f").

2. Switch (20) as defined in claim 1, wherein the circuit (21) comprises

- a generator (22) for, in an enable mode with the first control signal ("e") having a first value, generating the second control signal ("f") having a second value.

3. Switch (20) as defined in claim 2, wherein the circuit (21) further comprises

- a detector (23) for, in a disable mode with the first control signal ("e") having the second value, supplying the in/output signal ("y","z") to the generator for generating the second control signal ("f") having the first value in case of a value of the in/output signal ("y","z") being smaller than the first value and having the value of the in/output signal ("y","z") in case of the value of the in/output signal ("y","z") being larger than the first value.

4. Switch (20) as defined in claim 1, further comprising

- a further circuit (24) for in response to the first control signal ("e") and an in/output signal ("y","z") at an in/output of the switch (20) generating a backgate signal ("bg") destined for the second transistor (2).

5. Switch (20) as defined in claim 4, wherein the further circuit (24) comprises

- a further generator (25) for, in an enable mode with the first control signal ("e") having a first value, generating the backgate signal ("bg") having a value of the in/output signal ("y","z") and for, in a disable mode with the first control signal ("e") having a second value, generating the backgate signal ("bg") having the first value in case of a value of the in/output signal ("y","z") being smaller than the first value and having the value of the in/output signal ("y","z") in case of the value of the in/output signal ("y","z") being larger than the first value.

6. Switch (20) as defined in claim 2, wherein the generator (22) comprises a third (3) and a fourth (4) transistor of which first main electrodes are coupled to each other and second main electrodes are coupled to each other, which first main electrodes are further coupled to a first main electrode of a fifth transistor (5), which second main electrodes are further coupled to first main electrodes of a sixth (6), seventh (7) and eighth (8) transistor for generating the second control signal ("f"), with a control electrode of the third transistor (3) being coupled to first main electrodes of a ninth (9) and a tenth (10) transistor, with second main electrodes of the seventh (7), eighth (8) and tenth (10) transistor being coupled to each other, with a control electrode of the seventh transistor (7) being coupled to the first main electrode of the seventh transistor (7), and with control electrodes of the fifth (5), sixth (6), ninth (9) and tenth (10) transistor receiving the first control signal ("e") or a derived version ("$\bar{e}$") thereof.

7. Switch (20) as defined in claim 6, wherein a detector (23) comprises an eleventh (11) and a twelfth (12) transistor of which first main electrodes are coupled to each other for receiving the in/output signal ("y","z") or a derived version thereof, with a second main electrode of the eleventh transistor (11) being coupled to a control electrode of the twelfth transistor (12) and to a first main electrode of a thirteenth transistor (13), with a second main electrode of the twelfth transistor (12) being coupled to a control electrode of the eleventh transistor (11) and to a first main electrode of a fourteenth transistor (14) and to the second main electrodes of the seventh (7), eighth (8) and tenth (10) transistor, with control electrodes of the thirteenth (13) and fourteenth (14) transistor receiving the first control signal ("e") or a derived version ("$\bar{e}$") thereof.

8. Switch (20) as defined in claim 7, wherein a further generator (25) comprises a fifteenth (15) and a sixteenth (16) transistor of which first main electrodes are coupled to each other for receiving the in/output signal ("y","z") or a derived version thereof and second main electrodes are coupled to each other and to a first main electrode of a seventeenth transistor (17) for generating a backgate signal ("bg"), with a second main electrode of the seventeenth transistor (17) being coupled to a first main electrode of an eighteenth transistor (18), with control electrodes of the fifteenth (15), sixteenth (16) and seventeenth (17) transistor receiving the first control signal ("e") or a derived version ("$\bar{e}$") thereof, and with a control electrode of the eighteenth transistor (18) receiving the in/output signal ("y","z") or a derived version thereof.

9. Switch (20) as defined in claim 8, wherein the second transistor (2) is a PMOS having a backgate for receiving the backgate signal ("bg"), with the third transistor (3) being a PMOS having a backgate coupled to its second main electrode, with the seventh (7) and eighth (8) transistor each being a PMOS having a backgate coupled to its first main electrode, with the tenth (10) transistor being a PMOS having a backgate coupled to its first second electrode, with the eleventh (11) and twelfth (12) transistor each being a PMOS having a backgate coupled to its first main electrode, with the fifteenth (15) and seventeenth (17) transistor each being a PMOS having a backgate coupled to its second main electrode, with the eighteenth (18) transistor being a PMOS having a backgate coupled to its first main electrode, and with all other transistors (1,4,5,6,9,13,14,16) each being a NMOS.

10. Apparatus (30) comprising a switch (20) as defined in claim 1; and further comprising a first stage (26) coupled to a first in/output (Y) of the switch (20) and a second stage (27) coupled to a second in/output (Z) of the switch (20).